29. The method of claim 26 further comprising of adhering a third chip resistor to the second chip resistor with a second glass encapsulant.

30. The method of claim 26 wherein the glass encapsulant is glass frit.

31. The method of claim 26 wherein the first chip resistor and the second chip resistor are thick film resistors.

32. A method of manufacturing a stacked power chip resistor comprising:

adhering with a glass encapsulant a first chip resistor having a first substrate and a first resistive element to a second chip resistor having a second substrate and a second resistive element;

connecting a first terminal of the first chip resistor to a first terminal of the second chip resistor with a first metal barrier; and

connecting a second terminal of the first chip resistor to a second terminal of the second chip resistor with a second metal barrier.

with the first metal barrier, and connecting a second terminal on the first chip resistor to a second terminal of the second chip resistor with a second metal barrier.

In the Claims

Please cancel claims 1-25 without prejudice.

Please amend claim 26 as follows:

26. (Amended)

A method of manufacturing a stacked power chip resistor comprising:

adhering a first chip resistor to a second chip resistor with a glass encapsulant;

connecting a first terminal of the first chip resistor to a first terminal of the second chip resistor with a first metal barrier;

connecting a second terminal of the first chip resistor to a second terminal of the second chip resistor with a second metal barrier.

Kindly enter the following new claims 29-32:

29. The method of claim 26 further comprising of adhering a third chip resistor to the second chip resistor with a second glass encapsulant.

30. The method of claim 26 wherein the glass encapsulant is glass frit.

31. The method of claim 26 wherein the first chip resistor and the second chip resistor are thick film resistors.

32. A method of manufacturing a stacked power chip resistor comprising:

adhering with a glass encapsulant a first chip resistor having a first substrate and a first resistive element to a second chip resistor having a second substrate and a second resistive element;

connecting a first terminal of the first chip resistor to a first terminal of the second chip resistor with a first metal barrier; and

connecting a second terminal of the first chip resistor to a second terminal of the second chip resistor with a second metal barrier.